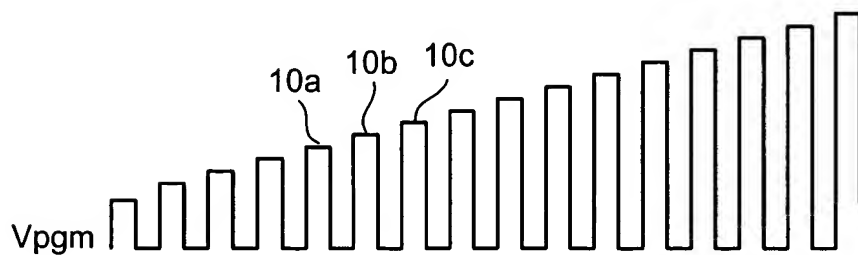


Fig. 1



of cells

Fig. 2

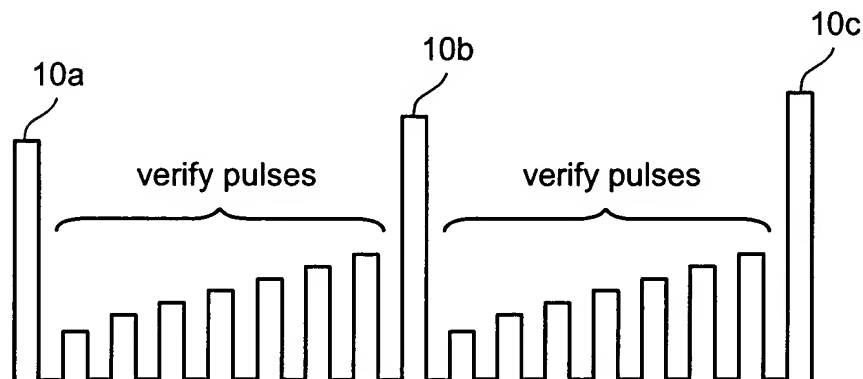
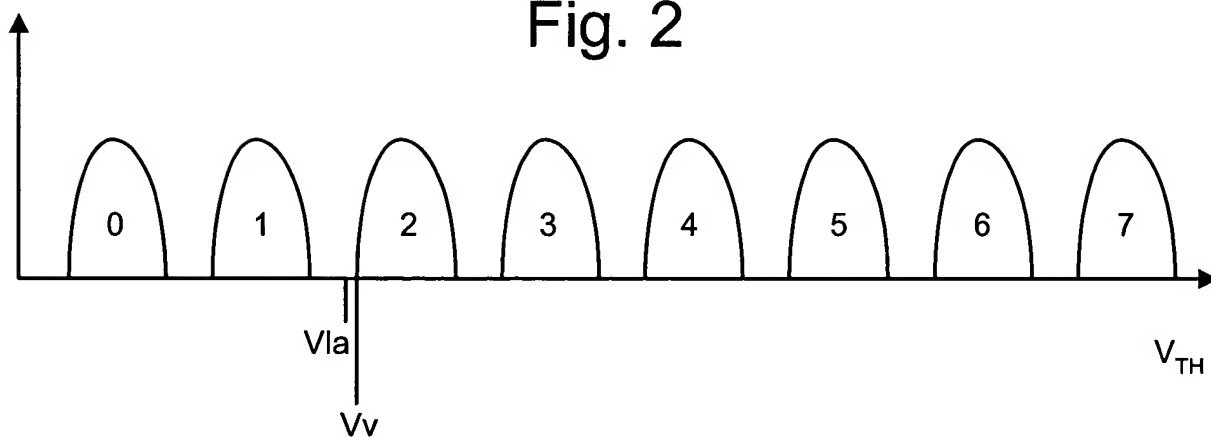
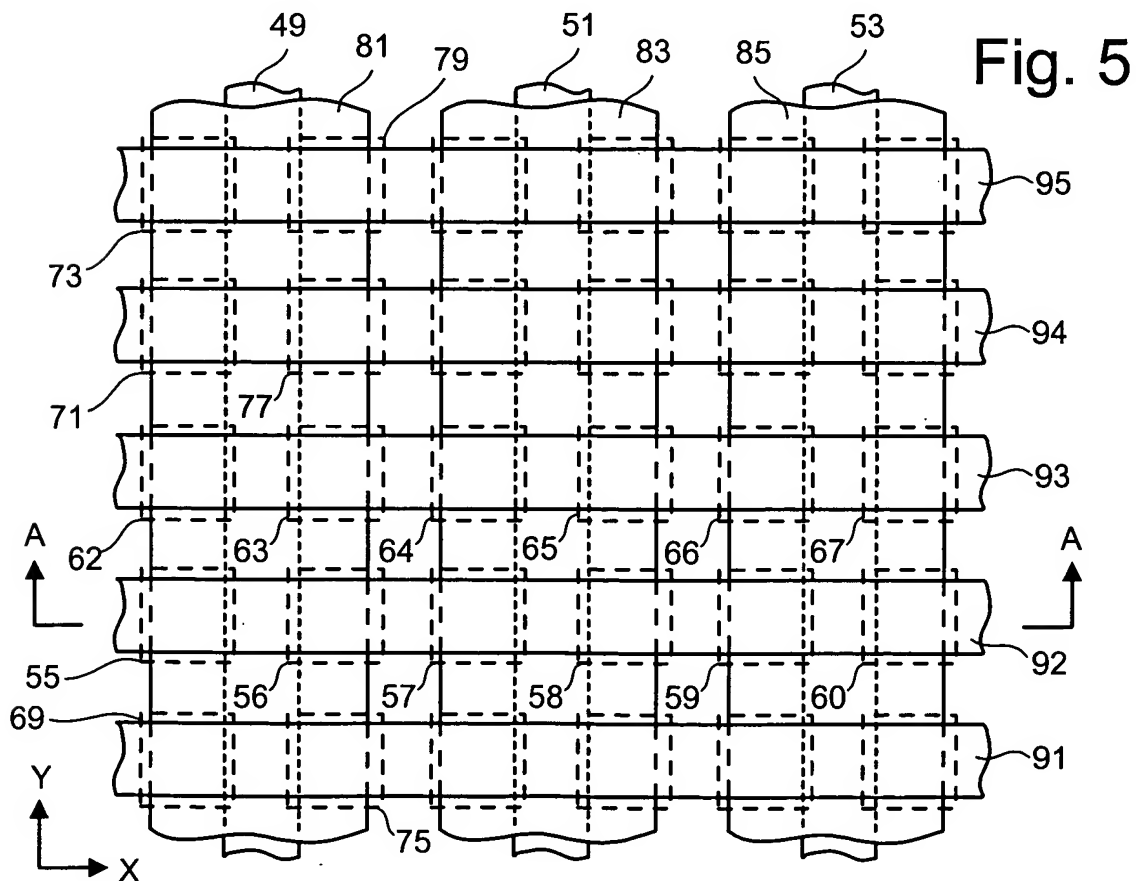
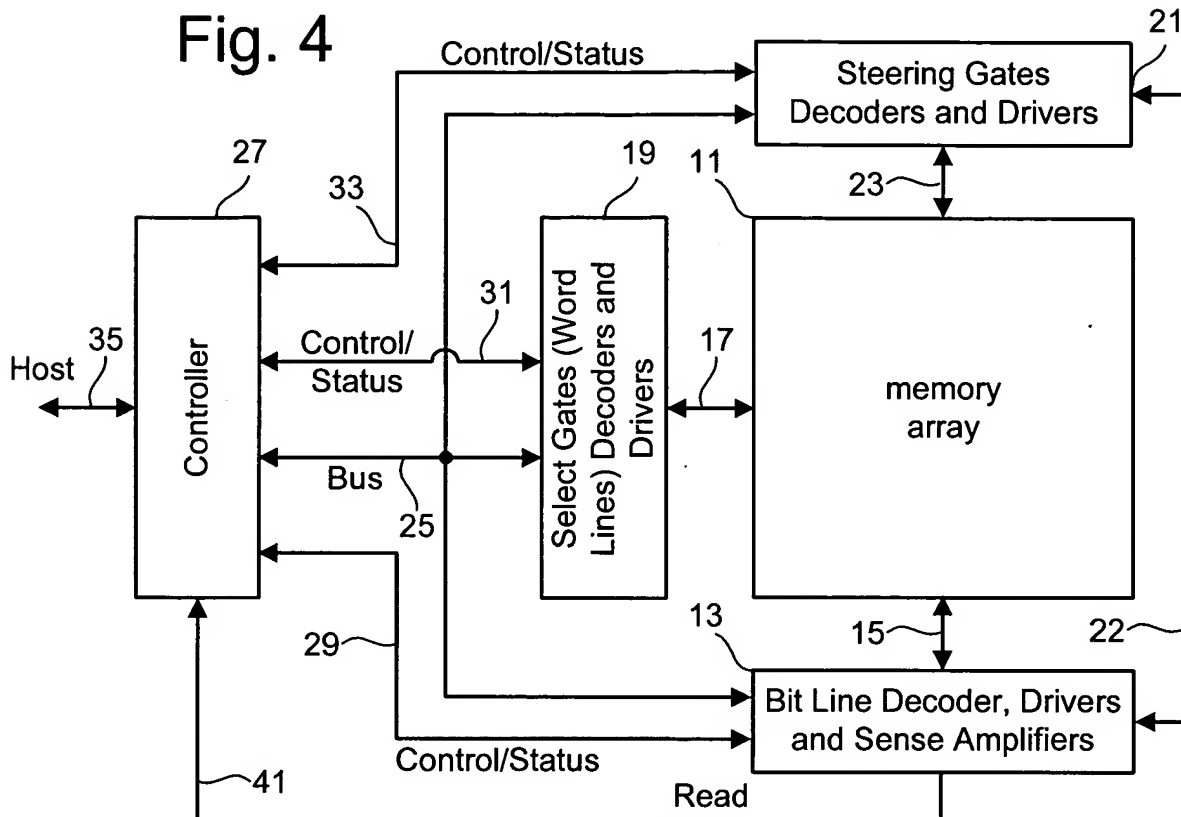


Fig. 3



[illegible]

Left Steering Gate

Select Gate (Word Line)

Right Steering Gate

55' 81' 56' 49' BL left

T1-Left T2

92' 99' 57' 58' 51' BL right

T1-Right

Fig. 8

FUNCTION BEING PERFORMED ON CELL	SELECT GATE (WORD LINE)	LEFT BIT LINE (BL - LEFT)	LEFT STEERING GATE	RIGHT STEERING GATE	RIGHT BIT LINE (BL-RIGHT)
(1) UNSELECTED ROW (2) ERASE (TO WORD LINE) (3) READ LEFT FLOATING GATE (4) READ RIGHT FLOATING GATE (5) PROGRAM LEFT FLOATING GATE (6) PROGRAM RIGHT FLOATING GATE (7) NO PROGRAM IN SELECTED ROW	0 V_E V_{SR} V_{SR} V_{SP} V_{SP} V_{SP}	X 5 0 1 5 0 0 5	X 0 V_M V_{BR} V_P V_{BP} X X	X 0 V_{BR} V_M V_{BP} V_P X X	X 5 1 0 0 5 0 5
(8) ERASE (TO CHANNEL) [WITH VOLTAGES OF BOTH THE p-well AND n-well EQUAL TO V_E , AND THE SUBSTRATE AT ZERO VOLTS]	V_{SE}	FLOAT	0	0	FLOAT

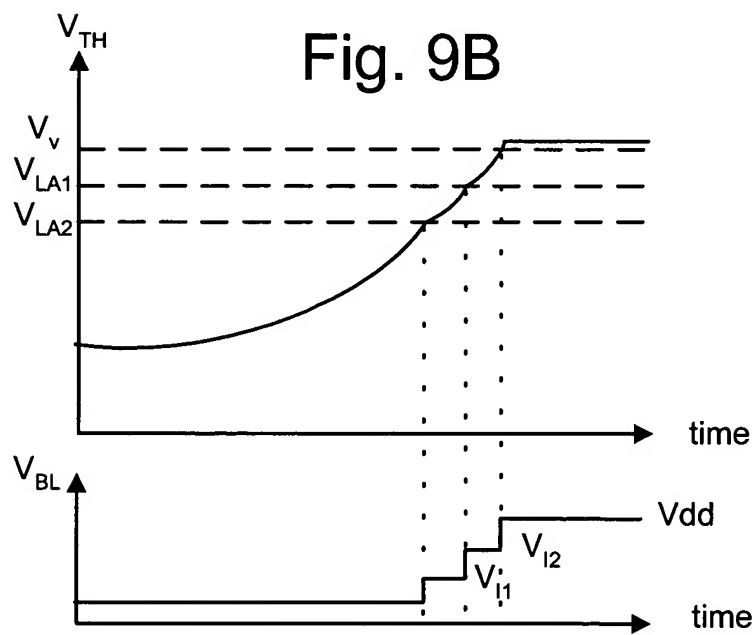
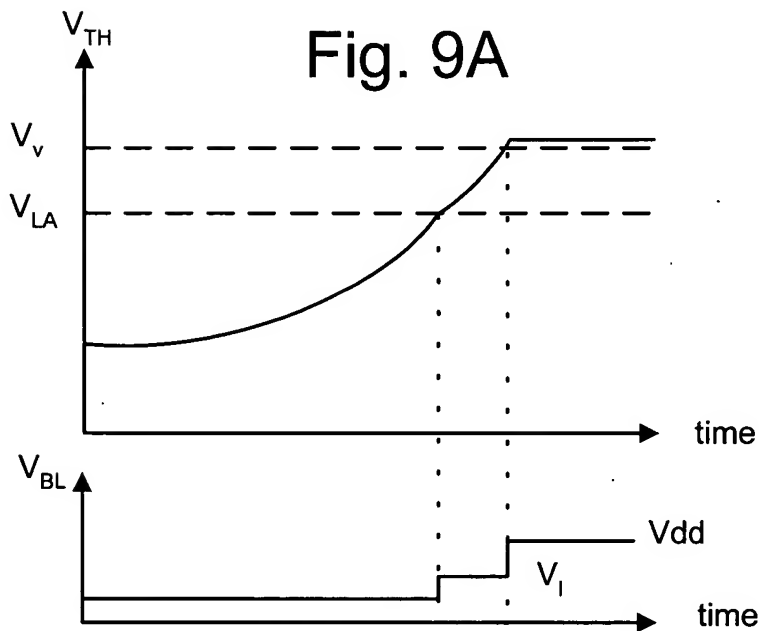
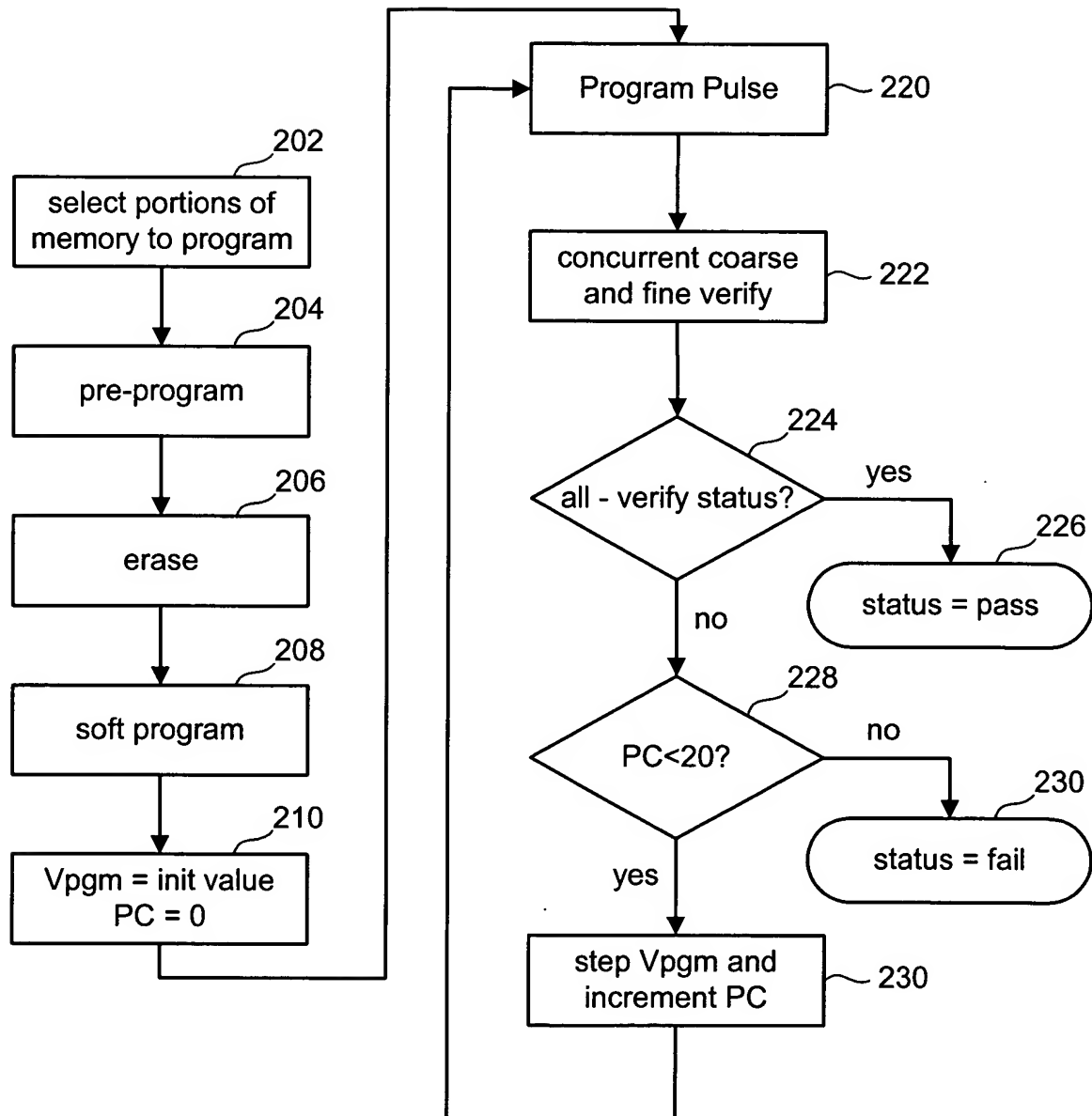


Fig. 10



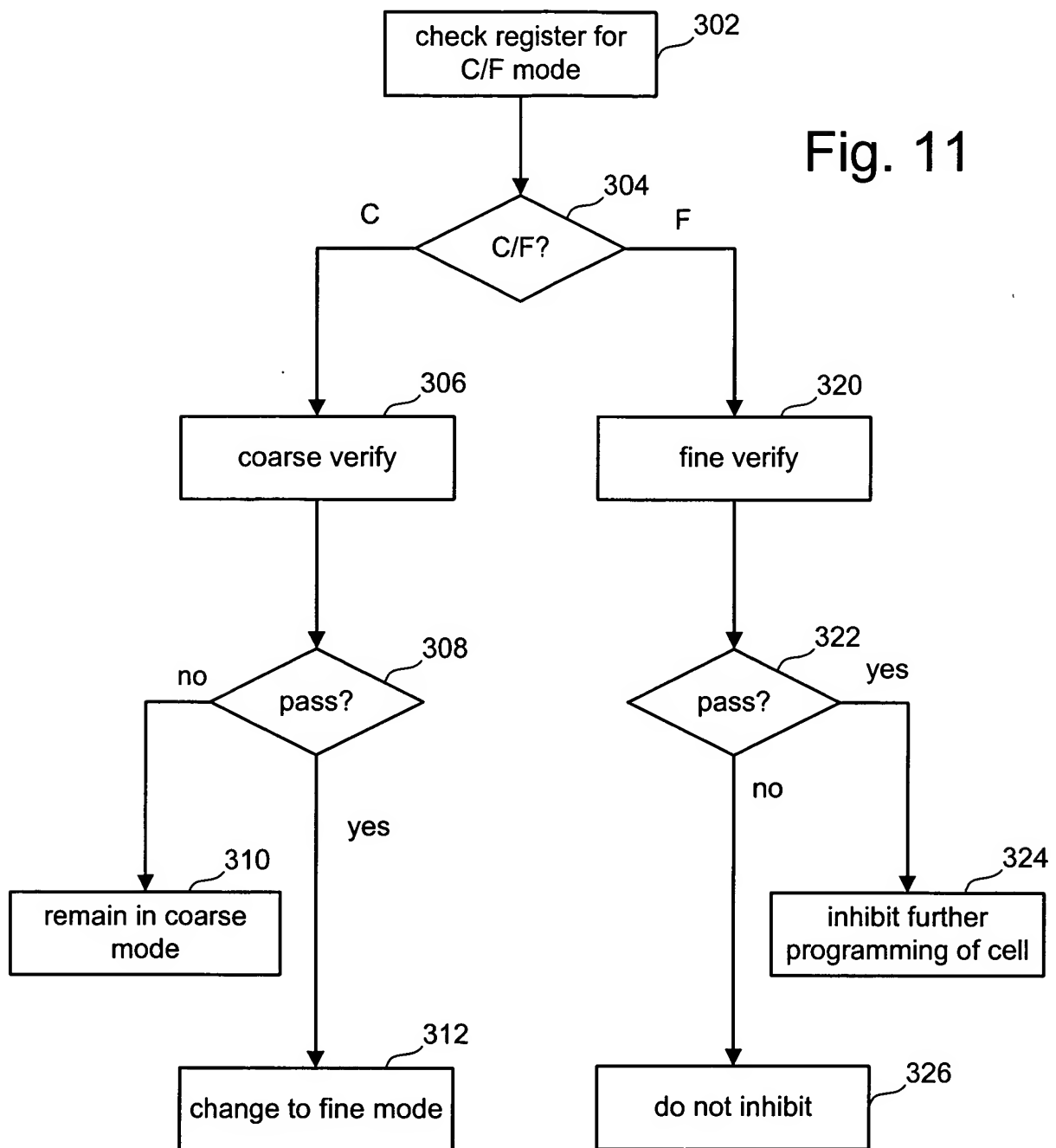


Fig. 12

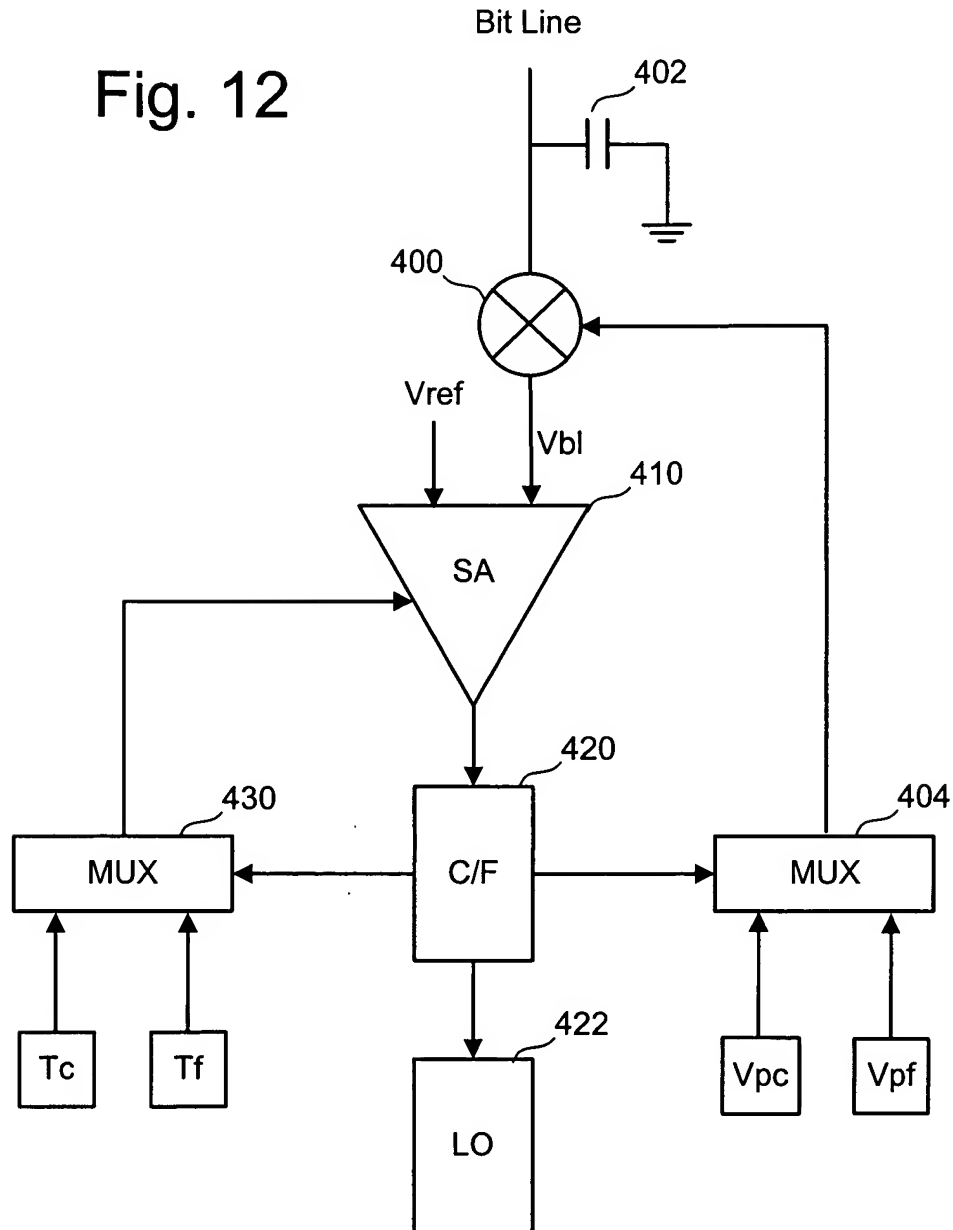


Fig. 13

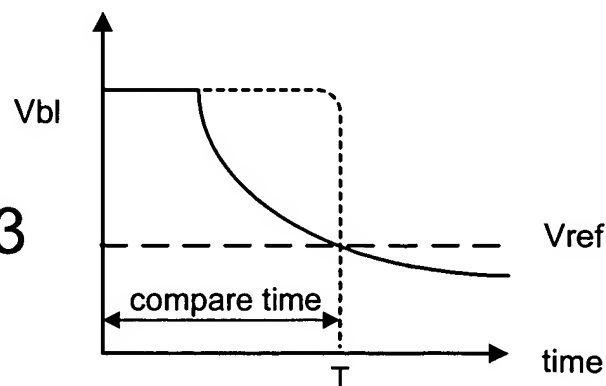


Fig. 14

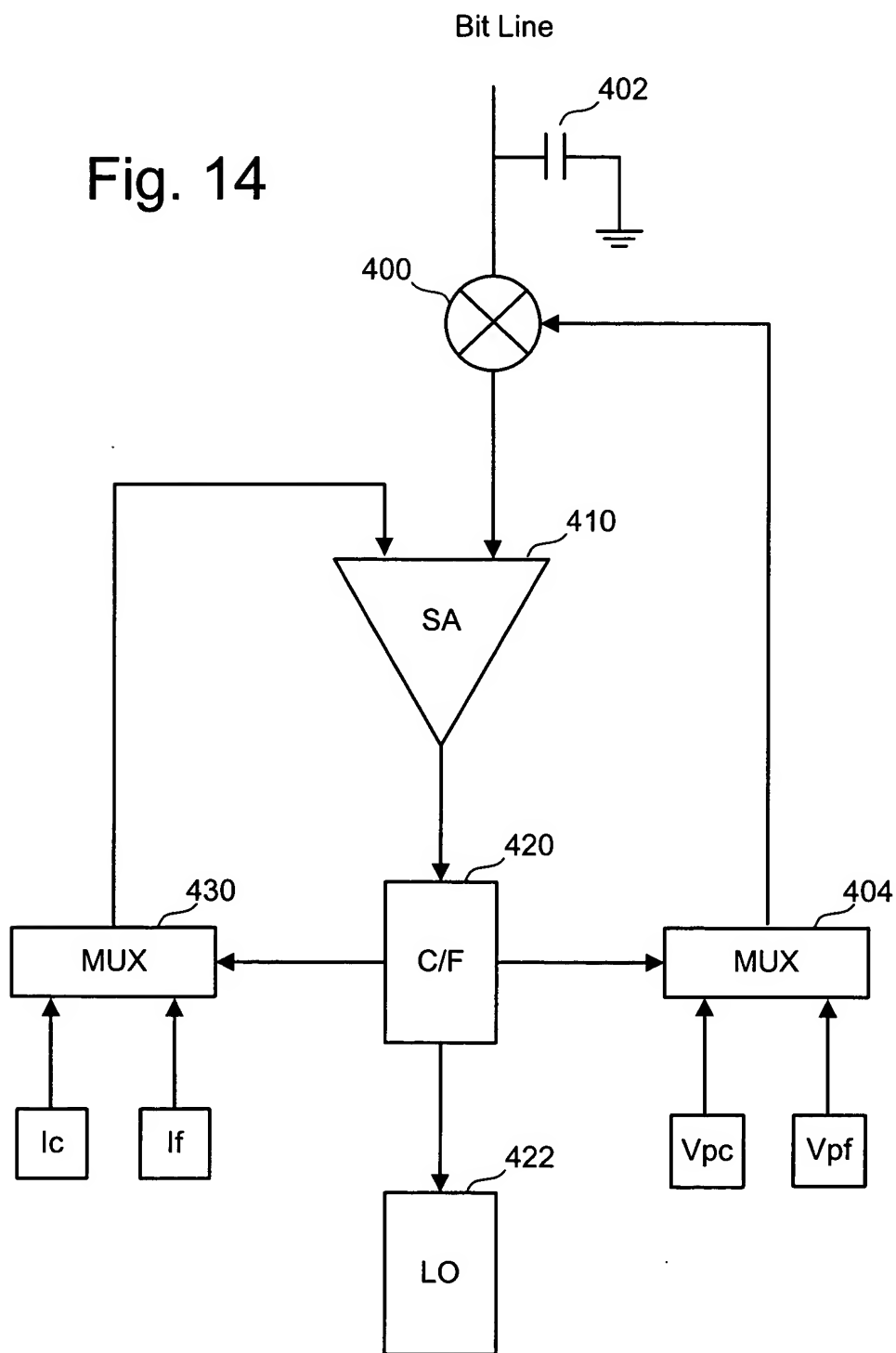


Fig. 15

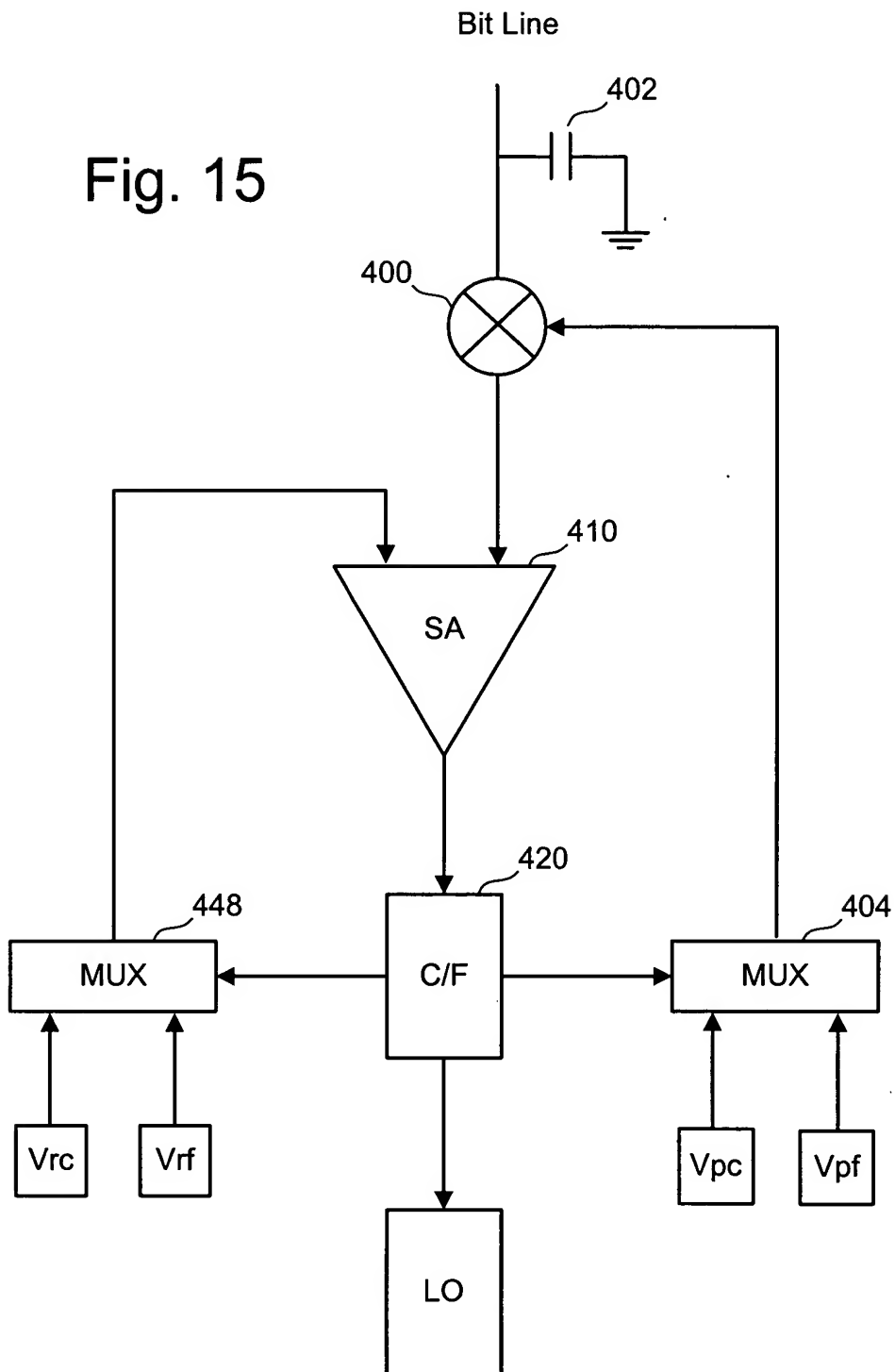


Fig. 16

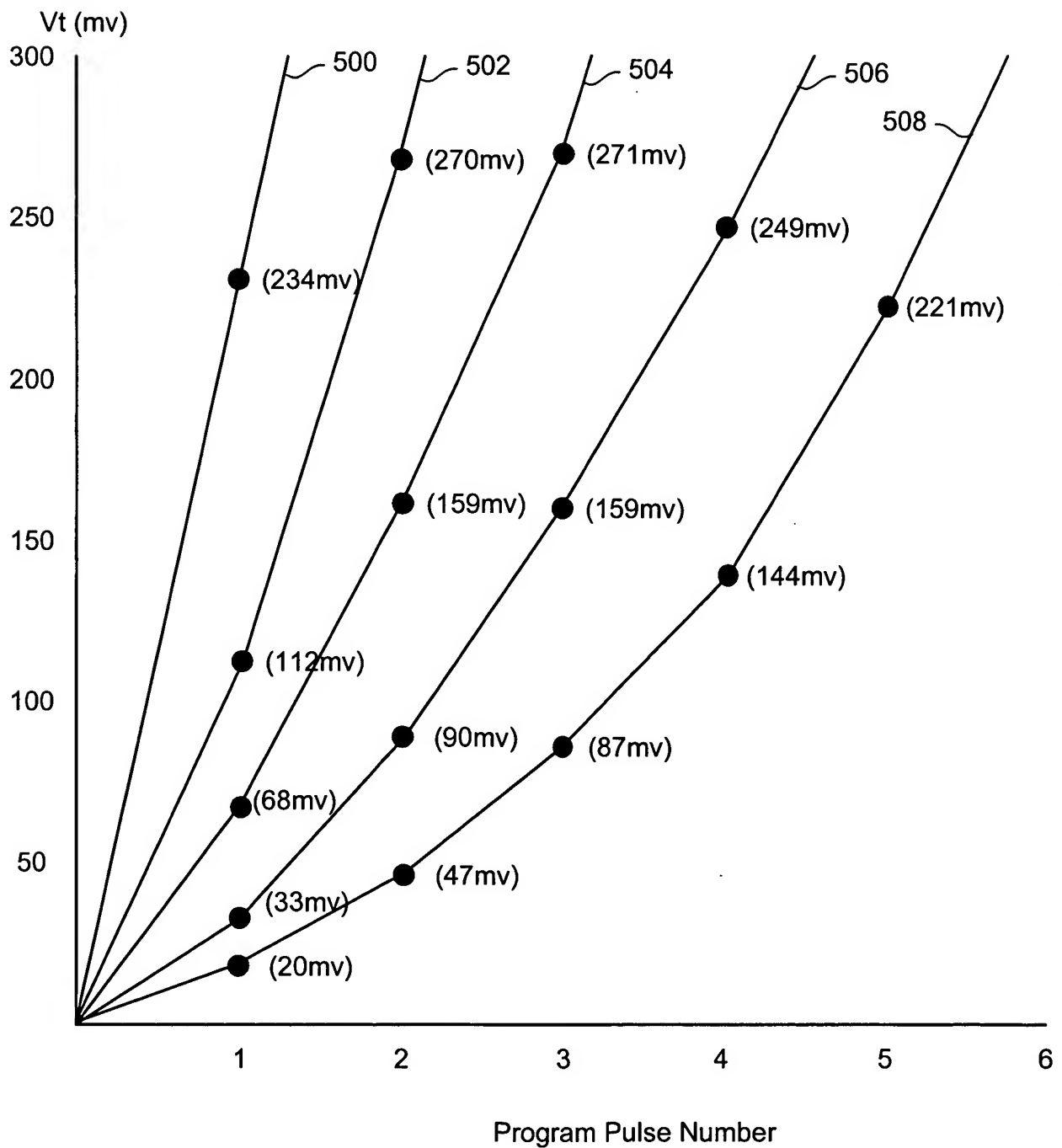


Fig. 17

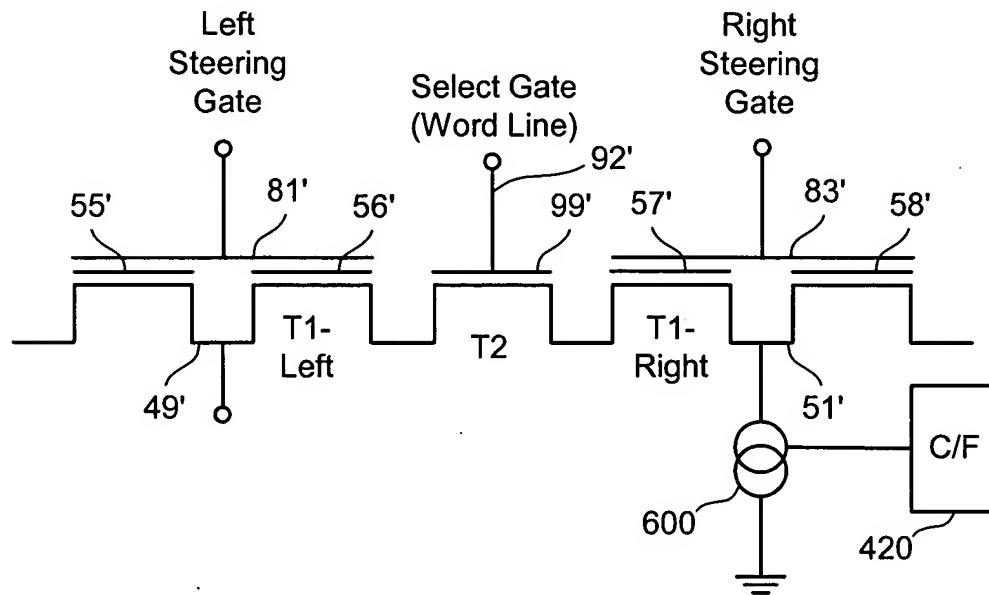


Fig. 18

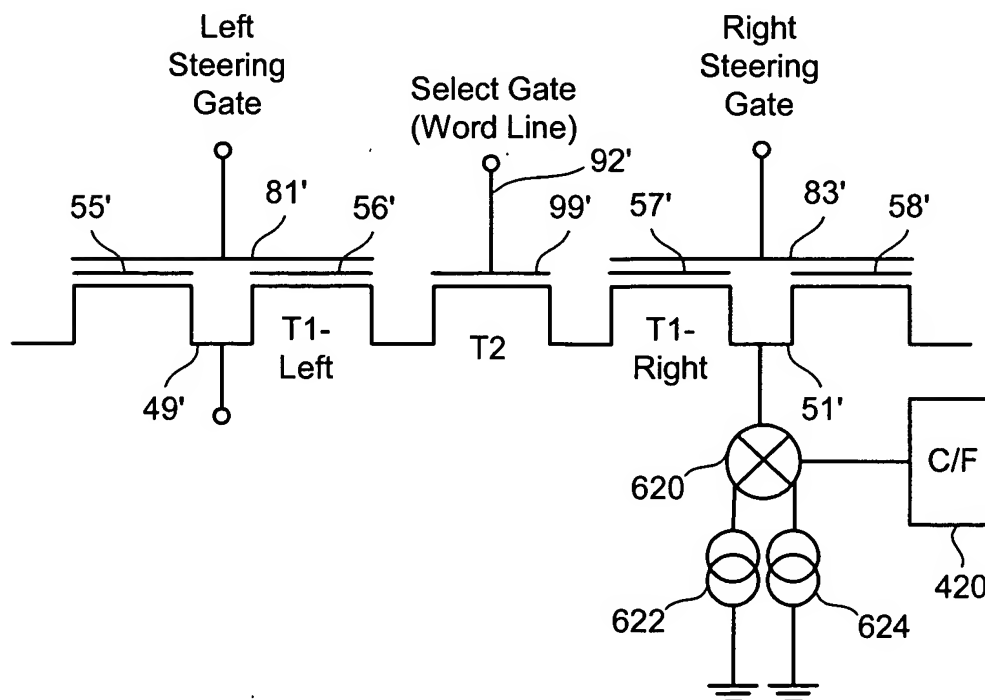


Fig. 19

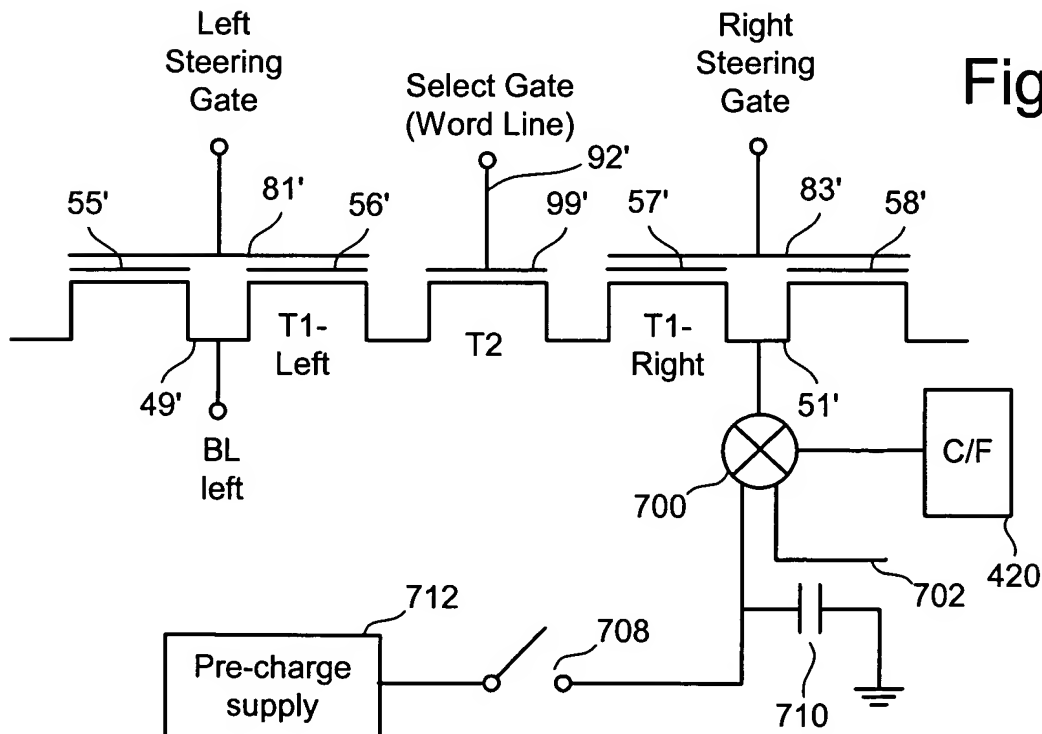
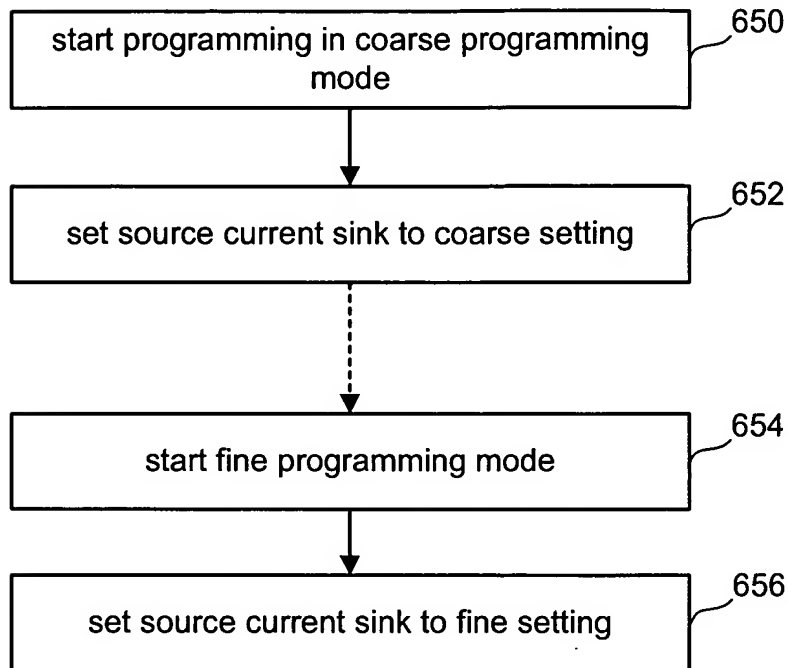


Fig. 20

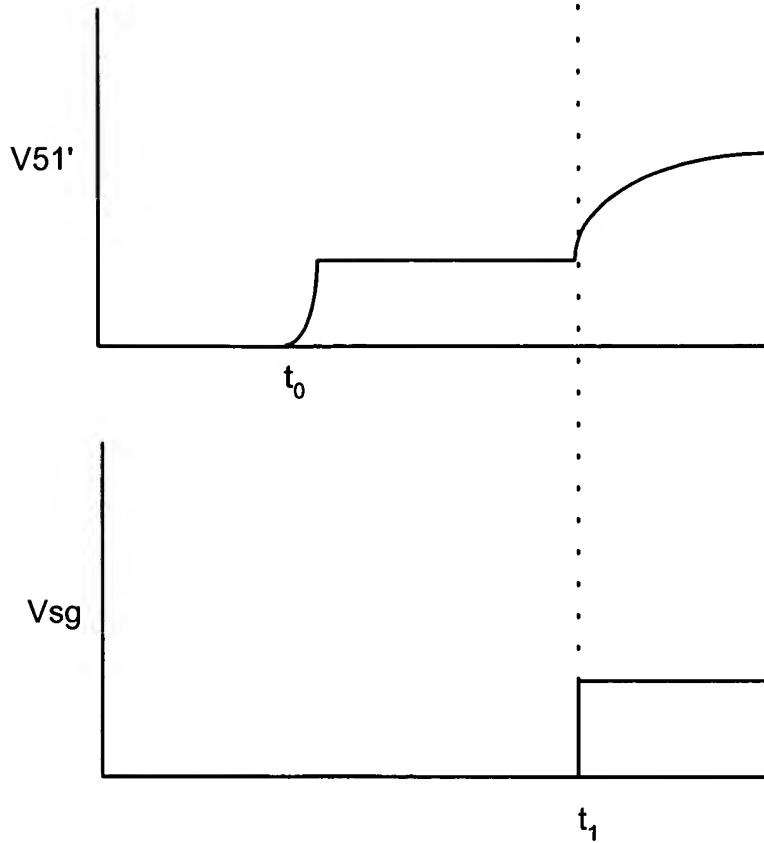


Fig. 21

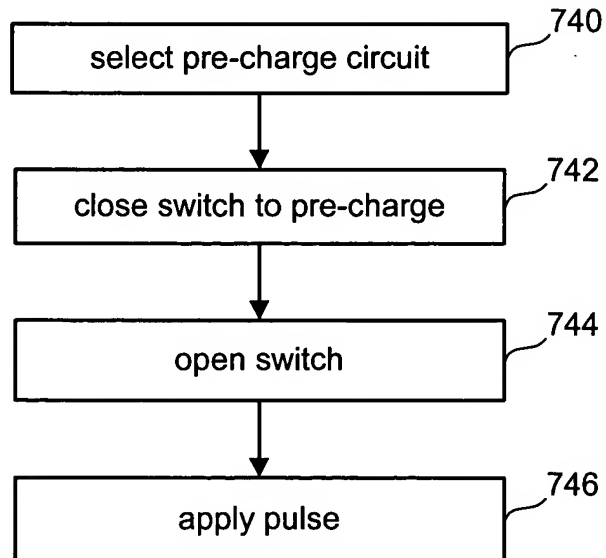


Fig. 22

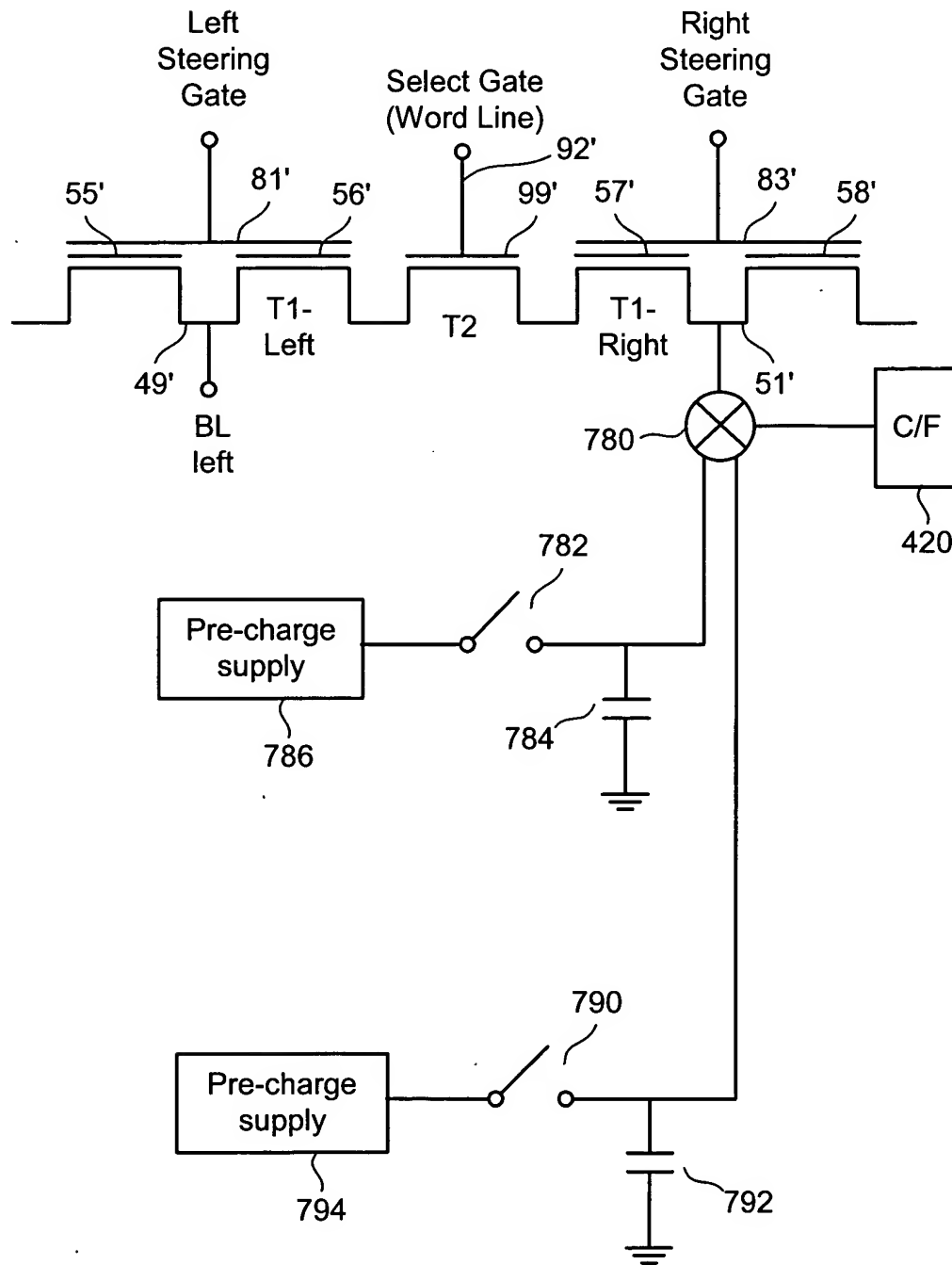


Fig. 23

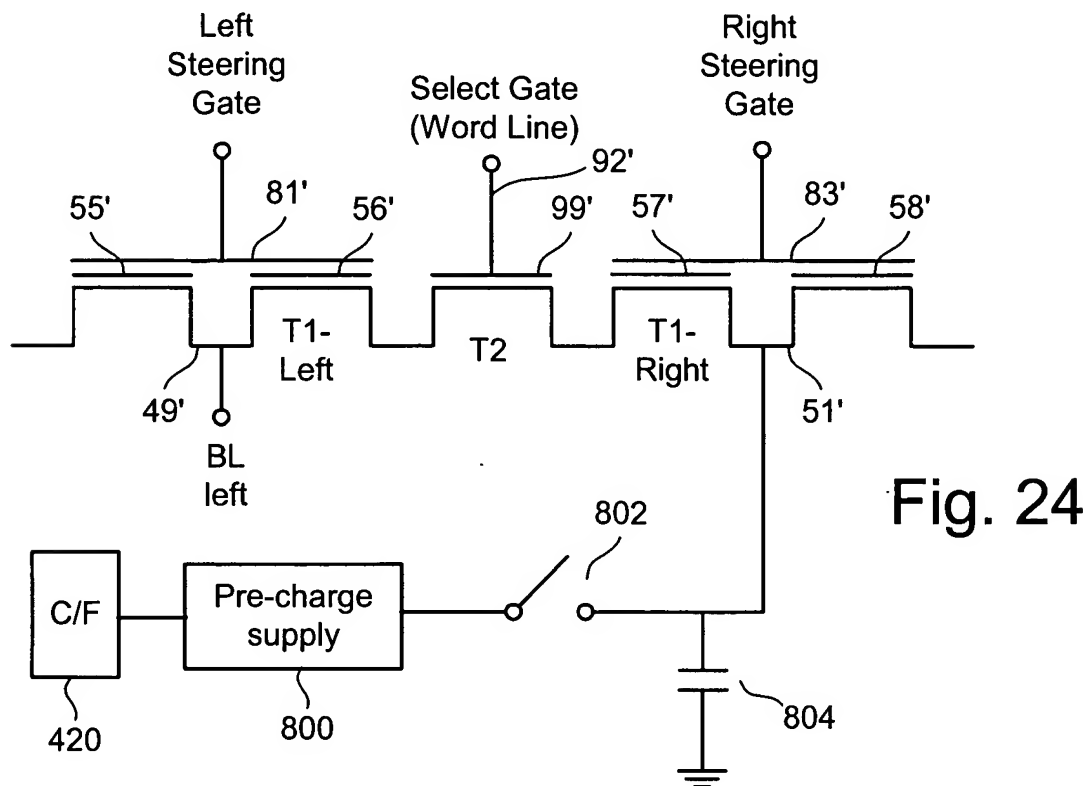


Fig. 24

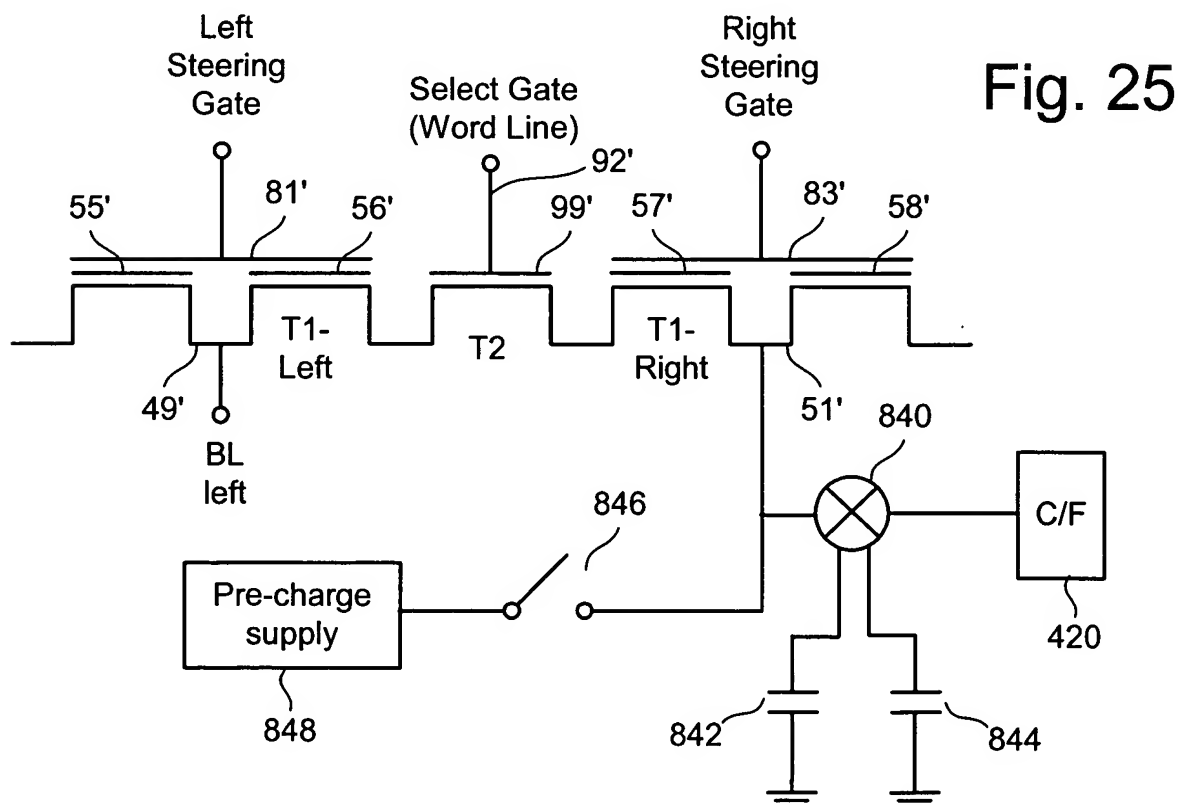


Fig. 25